JULY 1992

WRL
Technical Note TN-29

Electrical Evaluation Of The BIPS-0 Package

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July, 1992

Abstract

BIPS-0 is a fully-integrated bipolar processor chip with 100K ECL compatible inputs and outputs. Its external clock rate is about 100 MHz, with an on-chip clock rate of about 300 MHz.

The BIPS-0 chip is packaged in a 504 pin plastic pin grid array (PPGA) which provides 5 power planes, and two stripline signal layers designed to offer 348 signal lines with a characteristic impedance of 50 Ω. The chip's signal input pads include 50 Ω termination resistors.

In a system, the BIPS-0 package may be placed in a standard 504 pin zero insertion force (ZIF) socket which is soldered into a standard printed circuit board.

Using Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) techniques, the package trace impedance, impedance discontinuities due to the pins and bond wires, termination resistor resistance, signal edge rates, signal quality, crosstalk, and the performance degradation due to the ZIF socket were investigated. The results of this investigation will be used in the design of the package for BIPS-1 which will have an external clock rate of about 200 Mhz.

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1. Introduction

Incorporating research in the areas of computer architecture, bipolar VLSI CAD tools, and chip packaging and cooling, several members of Digital's Western Research Lab have designed and fabricated BIPS-0 and are working on BIPS-1.

BIPS-0 is a fully-integrated VLSI bipolar ECL processor chip, including an integer ALU, primary instruction and data caches, a write buffer, and a phase-locked loop based clocking system. Its external clock rate is about 100 MHz, with an on-chip clock rate of about 300 MHz.

BIPS-1 is an Alpha-compatible extension of BIPS-0, including a secondary BICMOS cache, floating-point, dual issue, and TLBs. Its external clock rate will be about 200 MHz, with an on-chip clock rate of about 1 GHz.

Both chips use 100K ECL compatible inputs and outputs and provide on-chip $50\,\Omega$ termination of signal input signals.

The BIPS-0 chip is packaged in a 504 pin plastic pin grid array (PPGA). There are five power planes, three provide Vcc (Ground), one provides the terminating voltage (-2.0), and one provides Vee (-5.2). Additionally, one of the signal layers includes Vee planes in the two quadrants which do not have signal lines. Each of the two signal layers is surrounded by power planes and is designed to provide $50\,\Omega$ stripline transmission lines. Given our edge rates (200 ps) and clock frequencies (200 MHz), transmission lines are essential to maintain signal quality.

To facilitate chip debugging, several high-frequency analog signals must be observable on the packaged parts. To preserve an much signal fidelity as possible, on BIPS-0 we chose to mount subminiature RF connectors (*Nanohex*^{TM} manufactured by ITT Sealectro) directly on the package.

Instead of soldering the PPGA into the system CPU board, the BIPS-0 package may be placed in a standard 504 pin zero insertion force (ZIF) socket which is soldered into the printed circuit board (PCB). The ZIF socket allows easy CPU replacement and facilitates system testing, but degrades signal quality.

Results of the evaluation of the BIPS-0 package and the ZIF socket will guide the design of the BIPS-1 package. The remainder of this note describes this evaluation. Section 2 describes the techniques for package evaluation, section 3 describes connecting the equipment, section 4 describes what we want to measure, section 5 describes the results. This note ends with section 6 which concludes that the BIPS-0-style package and ZIF socket performance is quite good, and will be suitable for BIPS-1.

2. Evaluation Techniques

The three frequently used techniques for package evaluation are modeling, frequency domain measurements, and time domain measurements.

The first step in modeling is to determine the package's electrically distinct pieces (e.g. pins, package traces, bond wires, package bond pads, ground planes, chip input or output pads). Then, for passive pieces, the physical dimensions are used as input to field solvers, or measurements are made to estimate their electrical characteristics. For active pieces, device models are usually available. The accumulated information then serves as input to a circuit simulator, such as *spice*, which estimates time domain and/or frequency domain behavior. Modeling provides guidance during the design of the package, but can only estimate the actual performance of the completed package.

There are two subclasses of frequency domain measurements: low frequency RLC measurement and high frequency network analysis. Low frequency (about 1 MHz) measurements cannot detect such phenomena as ground plane resonances, skin effect, dispersion, and dielectric losses. High frequency (GHz) measurements require sophisticated fixturing and careful setup, calibration and a capable operator. Both techniques result in a model of the package which can then be investigated with a circuit simulator. They treat the package as a "lump" and are unable to resolve the impedance contribution of an individual part (e.g. pin, package trace) of the package. With signal rise times of 200 ps and a propagation velocity of 15 cm (6 inches) per nanosecond, rules of thumb (pp. 8, [5]) indicate that distributed effects begin with interconnect lengths of greater than 4 mm (0.2 inches), and lengths greater than 15 mm (0.6 inches) should be treated as transmission lines. Since the electrical path through the package is up to 40 mm (1.5 inches), lumped treatment is inadequate.

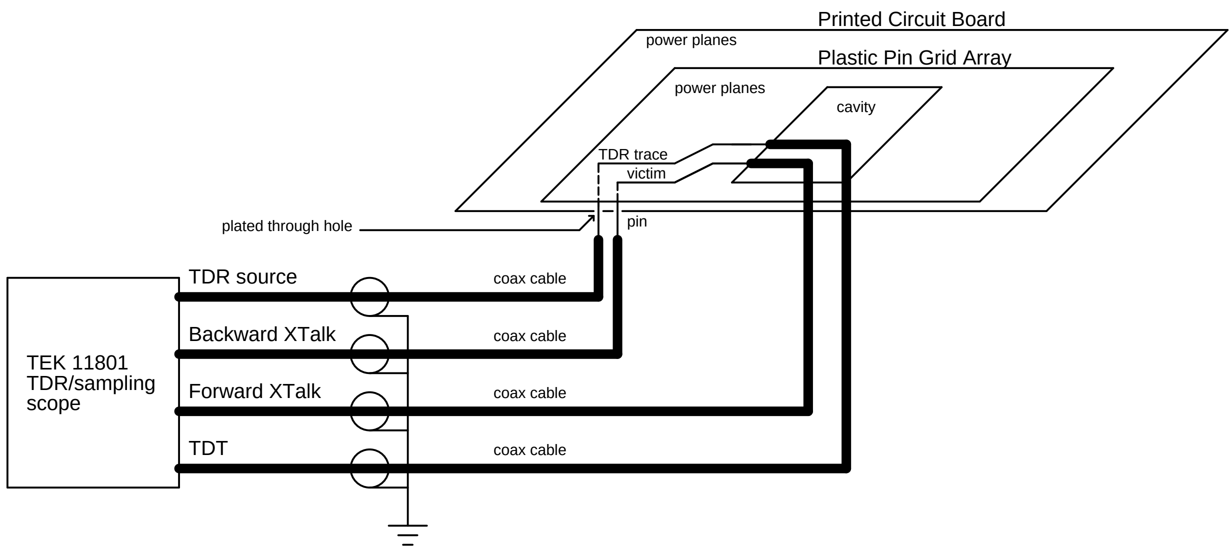

Figure 1: TDR Test Setup

We chose the third technique: time domain measurements, using time domain reflectometry (TDR), time domain transmission (TDT), and forward and backward crosstalk measurements with an oscilloscope. Figure 1 shows the test setup. The TDR source connection on the oscilloscope outputs a fast rise time voltage step (250 mV in 25 ps) and is also internally connected to one of the scope inputs. The other three connections are simply inputs to the scope. All of the scope inputs are internally terminated with 50 Ω to ground. The TDR and backward crosstalk coax cables are soldered to the chosen package pins; significant care was taken to provide low inductance connections from the coax center conductors to the signal pins, and from the coax shields to neighboring ground pins. The center conductors of the TDT and forward crosstalk coax cables were glued with silver-filled epoxy to the appropriate package bond pads. Their shields were spread out and soldered to an exposed portion of the package ground plane near the package signal pads. Here too, short, low inductance connections were made between the pads and the coax.

TDR works as follows. A voltage step is introduced into one end of a transmission line of characteristic impedance Z_o. If the step (called the incident wave, V_{inc}) encounters discontinuities in impedance (from Z_o to Z_x) as it travels along, part of the incident wave is reflected back (V_{ref}) towards the source. It can be shown (pp 237, [1]) that the ratio of V_{ref} and V_{inc}, called the reflection coefficient (ρ), is:

$$\rho = \frac{V_{ref}}{V_{inc}} = \frac{Z_x - Z_o}{Z_x + Z_o}$$

By considering the termination of a uniform transmission line, three cases are easily understood.

1. If the line ends in a short circuit, then Z_x is 0, ρ is –1, and the steady state voltage (after the reflection has propagated back to the TDR source) is 0.
2. If the line end is open, then Z_x is ∞, ρ is 1, and the steady state voltage is $2V_{inc}$.
3. If the line is terminated with a pure resistance of Z_o, then ρ is 0, there are no reflections, and the steady state voltage is V_{inc}.

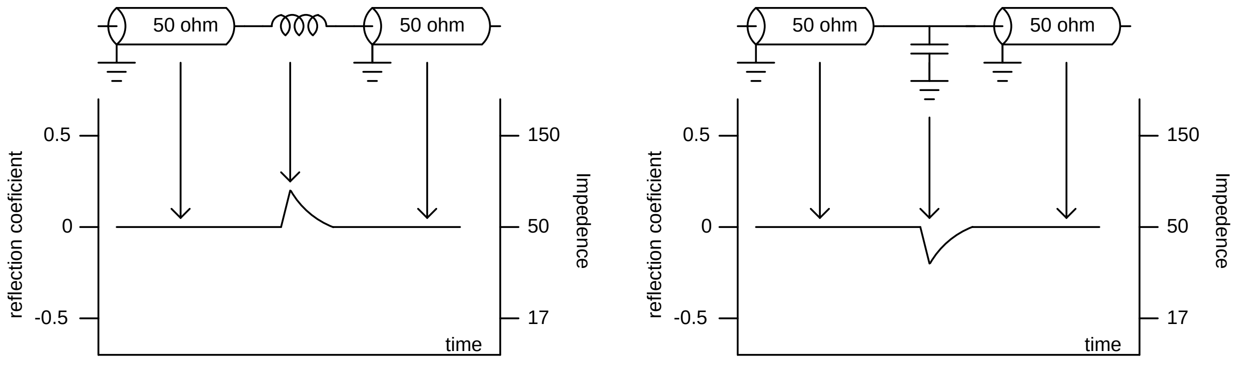

Figure 2: Oscilloscope Trace of TDR with Inductive and Capacitive Discontinuities

Some TDR oscilloscopes directly display the reflection coefficient, and assuming Z_o is $50\,\Omega$, display impedance along the trace. The left side of Figure 2 illustrates the TDR of a transmission line with a discontinuity with increased series inductance. The rise time of leading (rising) edge of the reflection is a lower bound on (but approximately equal to) the rise time of the incident wave. The trailing (falling) edge of the reflection is the exponential $L/(2\,Z_o)$ decay. The reflection is positive in sign as there is an impedance increase through the inductor.

The right side of Figure 2 illustrates the TDR of a transmission line with a discontinuity of shunting capacitance. The fall time of leading (falling) edge of the reflection is a lower bound on (but approximately equal to) the rise time of the incident wave. The trailing (rising) edge of the reflection is the exponential $2\,Z_o\,C$ decay. The reflection is negative in sign as there is an impedance decrease due to the capacitor.

As with other probing technologies, the resolution of the measurement depends on the wavelength of the probe. If the rise time of the TDR step is longer than the duration of the disturbance caused by the impedance discontinuity, the discontinuity may not be detected. This argues for the steepest possible TDR step, therefore permitting detection of small discontinuities. An alternative is to use TDR step rise times similar to the anticipated circuit signaling edge rates; only discontinuities significant to the expected circuit speeds with then be displayed. The equipment used in this experiment provides only fixed TDR rise times of around 25 ps. By the time that signal is fed through the connecting coax cables, its rise time is about 70 ps (determined through cable loopback to the scope). Our BIPS-based CPU boards use Motorola *ECLinPS* [4] parts to drive the BIPS inputs. These drivers have rise times around 300 ps, but the signal edges are degraded somewhat by the connecting printed circuit board (PCB) traces. The BIPS chip output pads driving the bond wires have rise times around 200 ps. Thus the TDR edge rates are considerably faster than the signals which will be presented to the package.

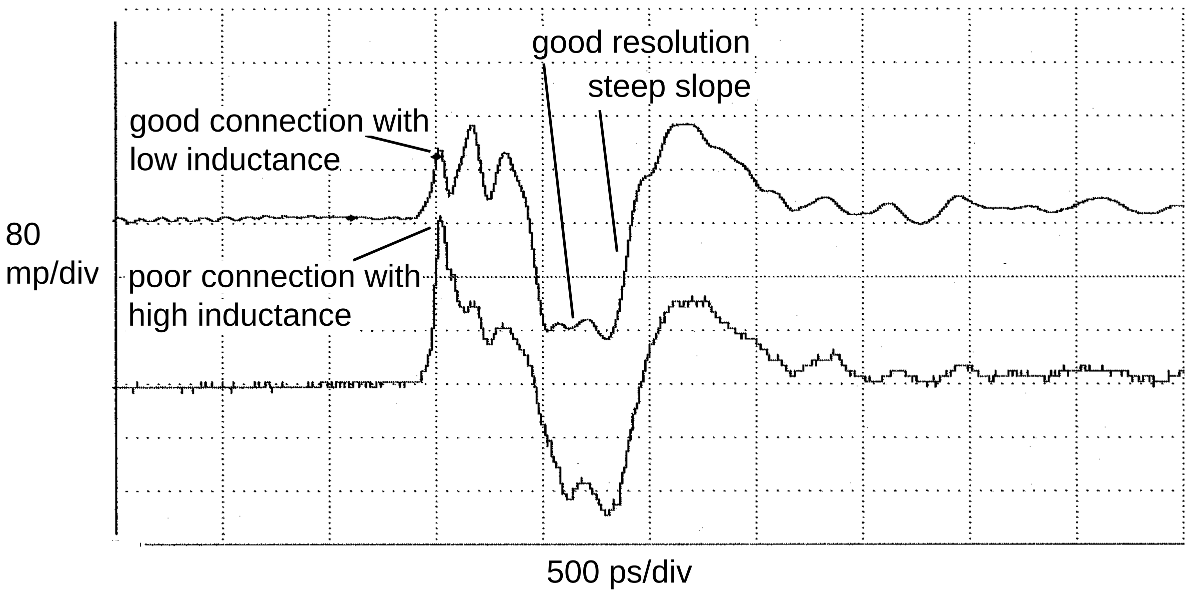

Figure 3: TDR Quality and Connections

Impedance discontinuities in a transmission line can be modeled by two transmission lines connected by a series inductance and shunting capacitance. Discontinuities behave as low pass filters with a cut-off frequency dependent on the characteristics of the discontinuity. Frequency components of the transiting signal near to and higher than the cut-off are attenuated, and the signal edge rates become slower. Signal rise times of 200 ps have a bandwidth of about 2 GHz (pp. 66, [3]). A series inductor of about 3 nh or shunt capacitance of about 3 pf in a 50 Ω transmission line creates a low pass filter with a cut-off frequency around 2 GHz. For TDR, this has two major implications. First, the connections between the scope’s coax and the device under test must be electrically "clean": discontinuities must be significantly smaller than those of the package. Second, TDR measurements beyond a large package impedance jump will be made with a slower step, so resolution will suffer. Figure 3 shows TDR measurements of a good coax-to-pin connection, and one poor connection. It illustrates the effects of a large impedance jump on the TDR resolution beyond the jump. If there are no reflections, TDR reveals no information on the edge rate of the transmitted signal.

TDR does not show signal quality (e.g. 20% to 80% edge rate, shape of the edge, ringing), but TDT does. TDT consists simply of introducing a signal with a steep edge to the input end of the transmission line under test, and inspecting the signal at the output end. TDT also permits measurement of propagation delays.

Direct cross talk measurements may be made by connecting to both ends of a package trace adjacent to the one carrying the TDR pulse.

3. Making the connection - how suitable are RF connectors?

Connecting the oscilloscope coax cables to the package turned out to be trickier than expected. Fortunately one of the major advantages of TDR is that you can determine the quality of the coax connection to the device under test directly using TDR. We first tried a conventional approach: PCB-mounted SMA and Nanohex connectors. These connector families are used to carry signals up to about 20 GHz. PCB-mount SMA connectors are about 6.5 mm (0.25 inch) square and require a 1.4 mm (0.056 inch) plated through hole finished diameter. PCB-mount Nanohex connectors are about 4 mm (0.16 inch) square and require a 0.9 mm (0.036 inch) plated through hole finished diameter.

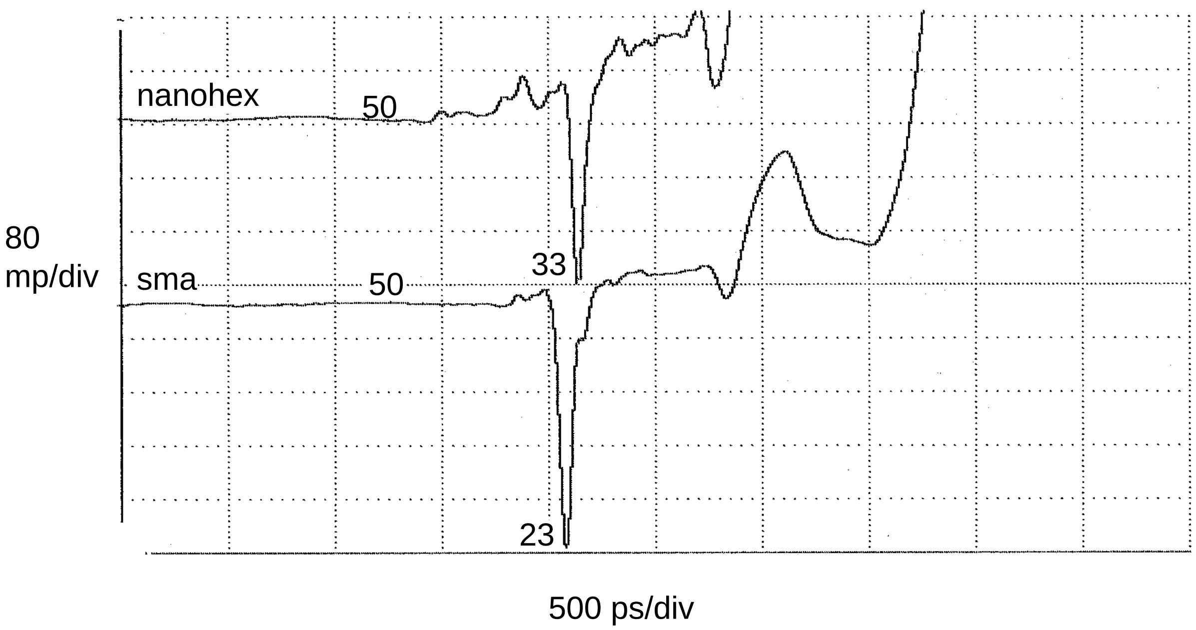

Figure 4: TDR with Nanohex and SMA connectors

Provisions were made for mounting 6 Nanohex connectors on the surface of the BIPS-0 package to monitor certain high frequency chip signals (e.g. on-chip clock). The upper trace of Figure 4 shows a TDR of a Nanohex connector soldered onto the BIPS-0 package. The BIPS-0 test cpu board used several SMA connectors for high frequency digital inputs and outputs (e.g. external board clock input). The lower trace shows a TDR of an SMA connector soldered into this PCB. Both of these reveal large impedance drops due to the capacitive plated through holes that the connectors are soldered into: from the 50 Ω coax cable down to 23 Ω for the SMA, 33 Ω for the Nanohex.

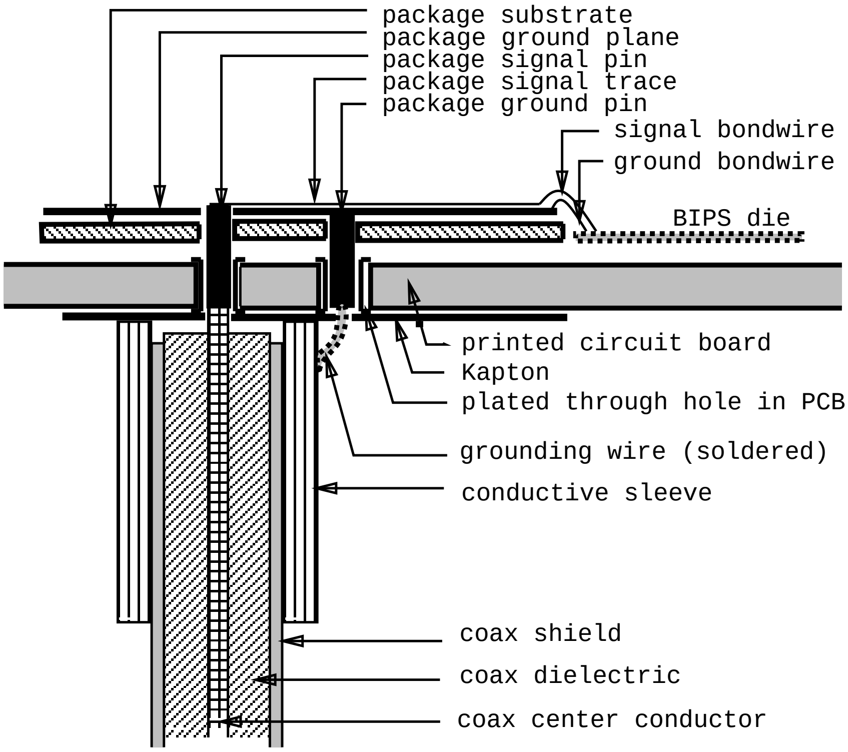

Figure 5: Soldered Coax to Pin Connection

The connectors performed inadequately: their impedance discontinuities obscured those of the package. To improve test signal transmission, we chose to do without the connectors and solder the coax directly to the device under test (see Figure 5). First, the package (or ZIF socket) was soldered into a test board which provided ground and power planes, and plated through holes (without signal traces) for the non-power pins. In the area of the connection, the lower surface of the PCB was covered with a thin insulating plastic film (*Kapton*^{TM}) to prevent shorting during hand-soldering (this worked much better than just relying on the solder mask). Holes were punched in the Kapton to provide access to the plated though holes. The center conductor of the coax was soldered directly to the bottom of the package (or ZIF socket) pin, where it protruded through the test PCB. The coax shield was surrounded with a conductive sleeve which was then lowered over the center conductor and soldered to neighboring ground pins.

Keeping the unshielded length of the coax center conductor short (about 2 mm) was critical to attaining a good signal fidelity. This soldered but-joint connection resulted surprisingly consistent inductive impedance jumps in the range of 53 to 58 Ω - quite acceptable. Figure 7 shows a TDR of a typical connection.

For TDT and cross-talk measurements it is necessary to connect to both the package pins, and to the package bond pads of adjacent package traces (see Figure 1). The bond pad spacing was about 150 microns (6 mils) so attaching coax to the adjacent bond pads was tricky. The approach we chose was to secure the coax to the package body with stiff wire, position the ends of the coax as close to the bond pads as possible, connect the coax center conductors to the bond pads with silver-filled epoxy, and solder the coax shields to the surrounding package ground plane. The photographs in Figure 6 show the rather messy remains of these connections upon

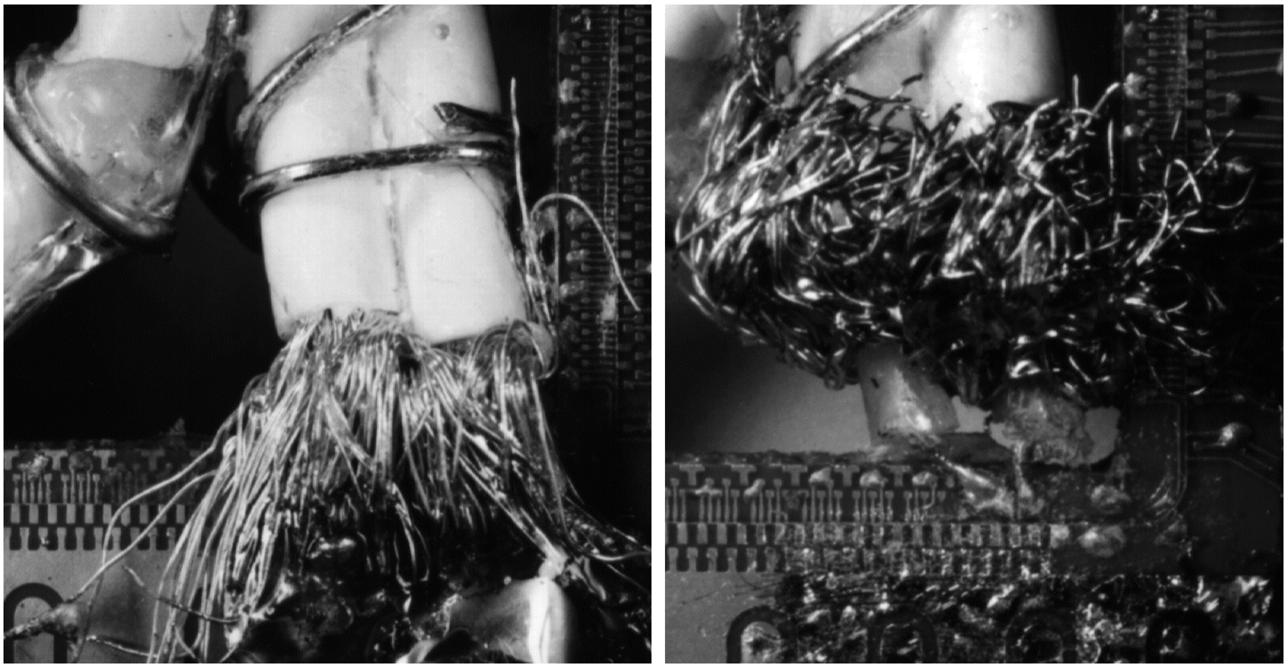

Figure 6: Coax to Bond Pad Connection

disassembly after testing. TDR measurements on these connections showed satisfactory performance, with an inductive discontinuity of about 70 Ω.[1]

4. Package Electrical Characteristics

The BIPS-0 PPGA [2] is built from copper-clad bizmaliamidetriazine (BT) laminates and pinned in a 25 x 25 array with 504 pins on a 100 mil grid. It provides 5 power planes, and two stripline signal layers designed to offer 348 signal lines with a characteristic impedance of 50 Ω. The chip's signal input pads include 50 Ω termination resistors. The package dielectric has a dielectric constant of about 4.5 and dissipation factor of around .015 at 1 GHz.

Digital Equipment Corporation typically packages its CPU parts in cofired alumina ceramic packages with tungsten conductors. These packages are strong and provide a hermetic environmental seal. The plastic package we chose offers better signal integrity due to the lower dielectric constant and conductor resistance. The dielectric constant for BT is 4.5, for alumina it is 9.5. The conductor resistance of 18 micron (0.7 mil, plated 1/4 oz. foil) copper is 1 $m\Omega$/square, for tungsten paste it is 8 $m\Omega$/square. A stripline transmission line consists of a sandwich of two conductive planes with a conductor embedded in a dielectric in the middle. The characteristic impedance of the transmission line depends on its inductance and capacitance per unit length. The capacitance depends on the dielectric used, and on the conductor width and its separation from the planes. The higher the dielectric constant, the further the stripline conductor must be spaced from the planes, or the narrower the conductor must be, to keep the capacitance

[1]Unfortunately the pad layout and cavity-down package precluded the use of devices such as standard Cascade microprobes.

down and therefore the characteristic impedance up. Increasing this spacing results in less capacitive coupling to the planes, but increased coupling to neighboring conductors thereby increasing crosstalk. Reducing the conductor width increases its resistance. The high signal line density on the package requires line widths at the minimum for tungsten paste (about 100 microns or 4 mils); reducing its width is not practical. It is difficult to make a ceramic package with high line density, 50 Ω impedance and low crosstalk. Theoretical treatments abound, [1] is a reasonable reference.

5. Measurement Results

Package characteristics of interest are package trace impedance, impedance discontinuities due to the pins and bond wires, termination resistor resistance, transmitted signal edge rates, edge shape, crosstalk, and the performance degradation due to the ZIF socket. The results of this investigation of the BIPS-0 package will be used in the design of the package for BIPS-1 which has a higher external clock rate of about 200 Mhz.

5.1. Package Impedances and On-chip Termination - TDR

Figure 7 shows overlaid TDR measurements of an input pin for 6 packages with a wire-bonded die and 1 package without a die. Various package components[2] and their impedances are identified. The packages were mounted in a ZIF socket which was soldered into the PCB described above. The input pads contain on-chip terminating resistors resulting in the (roughly) 50 Ω trailing ends of the TDR. The TDT results discussed in section 5.3 indicate that the TDR pulse rise time at the input pads is inadequate to determine the location or impedance of the chip pads or terminating resistors.

Figure 8 shows similar TDR measurements of an output pin on 6 packages, each of the packages held a wire-bonded die. The chip's (unterminated) output pads present a high impedance, resulting in the rise at the end of the TDR traces.

From these measurements we observed that the combined ZIF socket and pin inductive impedance jump was the largest discontinuity. The capacitive annular ring at the top of the pin was evident (see section 5.5 for details). The trace impedances were about $60\,\Omega \pm 3$. While the packages had been designed for 50 Ω, the package vendor had problems with resin bleed: while curing the resin under pressure, resin was squeezed out onto the bond pads. Bleeding was eliminated by reducing the pressure, however the resulting increased trace-to-plane distance also increased the trace impedance. The vendor has since overcome this problem so it is not expected to be an issue for BIPS-1.

BIPS-0 has an on-chip terminating resistor for each of its 200 inputs. Often the additional power dissipation of such resistors precludes their use on chips. With BIPS-0 dissipating about 100 Watts, the additional 4 Watts for terminating resistors was considered insignificant. In addition to reducing board parts count, on-chip terminators result in better signal integrity since the

[2] During TDR testing these can be identified by forcing impedance discontinuities, for example by shorting the top of the package pin to a nearby ground pin.

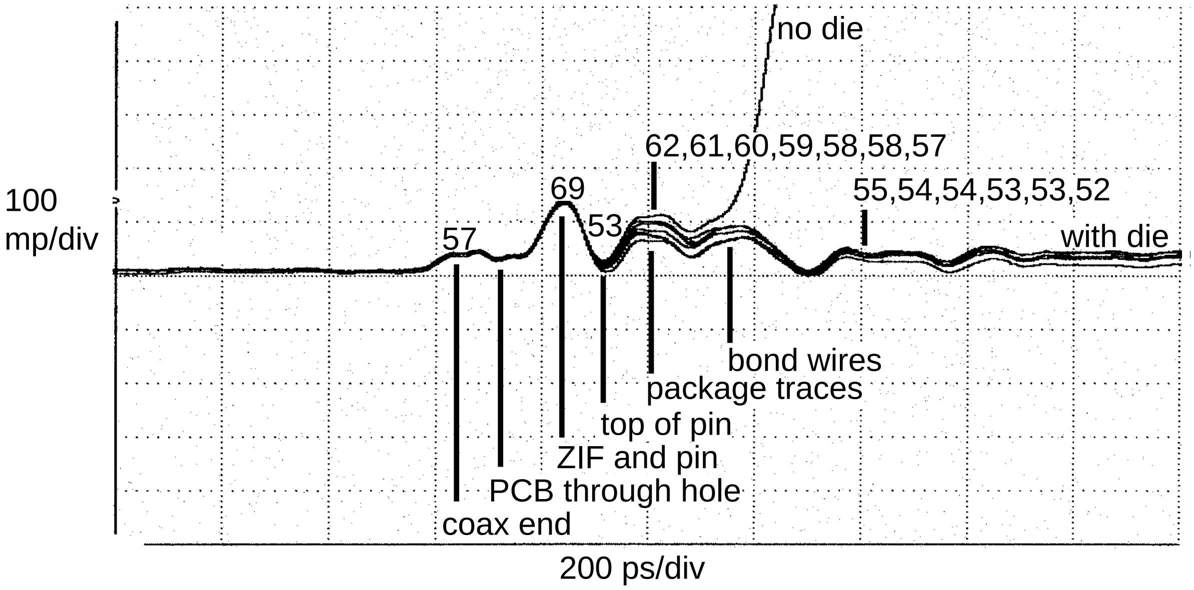

Figure 7: TDR of Input Pins

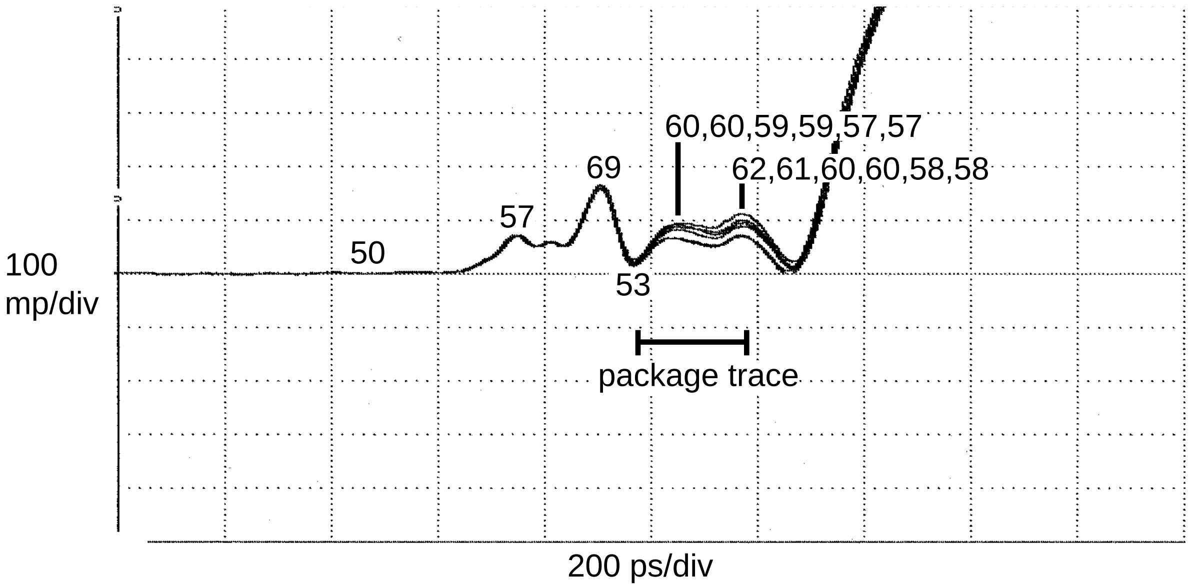

Figure 8: TDR of Output Pins

resistor is at the end of the signal line; the CPU is not a stub off the signal line. Measurements showed that the resistance of the on-chip terminating resistors was $53\,\Omega \pm 5$.

The collection of TDR measurements (10 pins on 15 packages = 150 TDRs) showed that the trace impedance was $60\,\Omega \pm 3$, with slight dips at the top of the pin and near the bond pads where the traces were crowded. The impedances were similar on both stripline signal layers of the package. The impedance depended primarily on the dielectric spacing, not on the proximity of adjacent traces. There was a small rise in impedance over the bond wires due to their self-inductance, and a small drop at the capacitive chip pad.

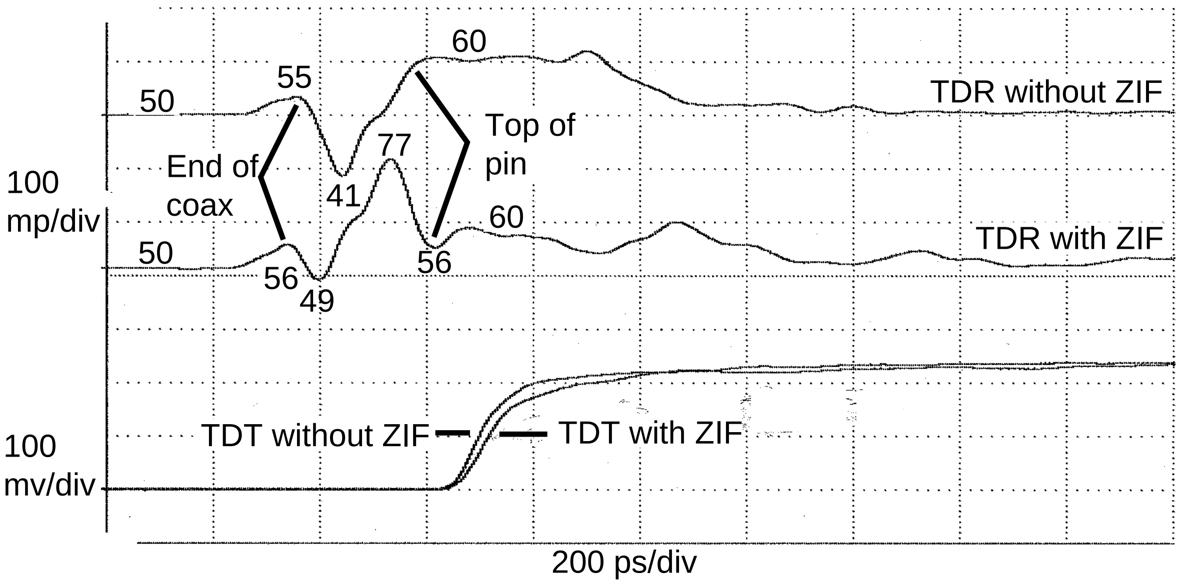

Figure 9: TDR and TDT with and without ZIF Socket

5.2. ZIF Socket Performance

Figure 9 compares two TDRs of the same pin on the same package. In one case, the package was soldered directly into the PCB (the upper TDR), in the other, the package was inserted in the ZIF socket (the lower TDR). The inductive impedance jump from the package pin and ZIF socket present in the lower TDR is absent from the upper trace. Instead, in the upper TDR, the capacitive plated through hole presented a bigger overall drop than that in the lower trace. Using the ZIF socket presented a bigger impedance discontinuity in the path between the PCB and the package trace, and degraded the signal rise time somewhat. This can be seen in the TDT traces below the TDRs, and will be discussed in the next section.

5.3. Edge Rates through Package - TDT

The rise time of a transmitted signal depends on many factors including: the rise time of the source signal, impedance discontinuities encountered during transit, conductor skin effects, dielectric losses[3] dispersion, reflections, and loading. Except for the effects of loading and bond wires, the impact of these factors may be directly observed by measuring the transmitted signal at the bond pads. The bottom traces in Figure 9 are an example of TDT. These traces show that, with the 250 mV swing and 25 ps rise time of the TDR source, the output swings 20 to 80% in about 120 ps with no ZIF socket and 145 ps with the socket.

[3]The longest package trace is about 1.5 inches, is 3 mils wide, and is in a stripline environment. Calculations (see chapter 6 of [1]) indicate that, for frequencies below 5 GHz, attenuation due to skin effect is less than 6% and attenuation due to dielectric losses is less than 4%.

Uncertainty as to the validity of directly extrapolating these measurements to expected rise times with the typical 750 mV 100K ECL swing led to us making TDT measurements using a pulse generator capable of variable swing (but not variable rise time) for the signal source. These results are contained in Table 10, and they indicate that ECL rise times of less than 150 ps can be accommodated with the ZIF socket and 125 ps without. This is better than required: the BIPS-1 chip pads will have edge rates no faster than 200 ps, and the ECLinPS devices on the CPU board have output edge rates around 300 ps (which will be even slower after traveling through the FR4 circuit board).

Input Swing +/- 2%	Input Rise Time +/- 5 ps	No ZIF Output Rise Time +/- 5 ps	With ZIF Output Rise Time +/- 5 ps
0.25	80	115	139
0.50	85	118	145
0.75	90	124	144
1.00	91	126	141
1.25	92	124	145
1.50	90	122	143
1.75	96	125	144
2.00	99	130	154
2.25	104	132	159
2.50	108	138	164

Figure 10: Rise Times as a Function of Swing

5.4. Crosstalk

Figure 11 shows an example of forward and backward crosstalk measurements. The TDR source was used as the excitation (on the *aggressor* trace), and the crosstalk measurements are on an adjacent (*victim*) trace. These two traces were parallel for approximately 28 mm (1.1 inches) or approximately 200 ps. Crosstalk current in the victim trace in the direction of the source end (the *near* end) of the aggressor is called backward crosstalk. Crosstalk current in the other direction (toward the *far* end) is called forward crosstalk [3].

As the pulse propagates down the aggressor trace, its signal is capacitively coupled into the victim trace, causing current (I_C) to flow from the point of coupling to both ends of the victim's trace. Coincident with capacitive coupling, the mutual inductance of the parallel lines also couples current (I_L) into the victim trace in the direction of backward crosstalk.

At the far end of the victim trace, the forward crosstalk is $I_C - I_L$. With a homogeneous dielectric, these cancel and no forward crosstalk should be observed.

The backward crosstalk is $I_C + I_L$, and is a function of the time (i.e. the distance divided by the signal propagation velocity) the victim and aggressor are adjacent, T_{prop}. The coupling begins where the two traces become close, and continues while the aggressor's edge travels to the far end (one T_{prop}). The coupled signal at the far end then takes another T_{prop} to return to the near end of the victim. Thus the duration of the backward crosstalk is $2\ T_{prop}$.

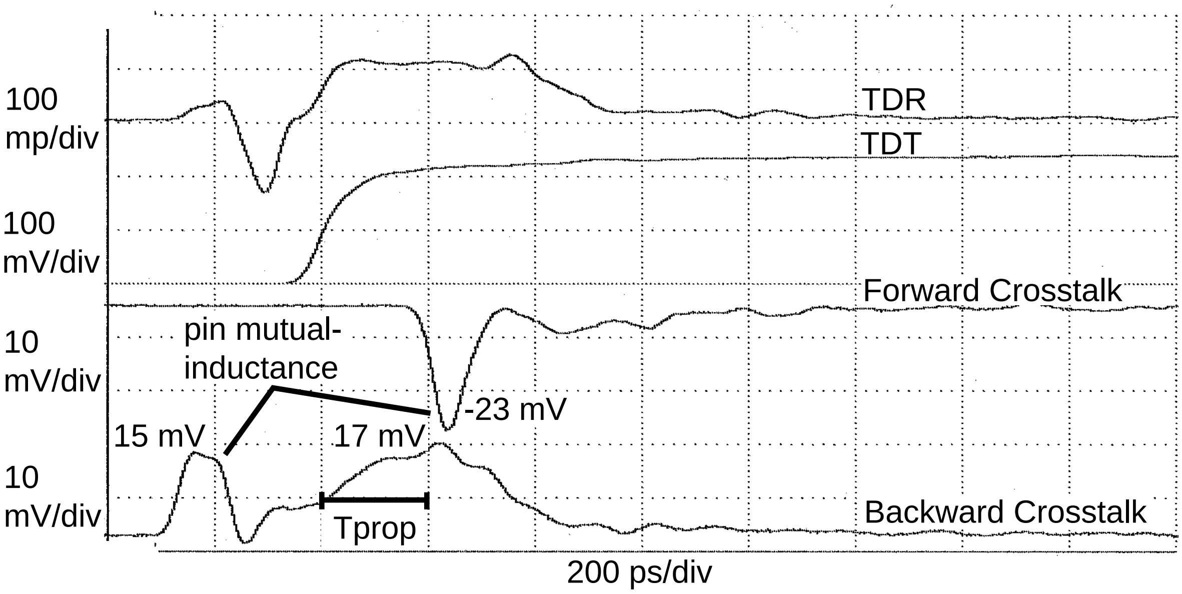

Figure 11: Forward and Backward Crosstalk

Figure 11 shows that there is about 20 mV (less than 10%) of forward crosstalk - the presence of any forward crosstalk was a surprise. Investigation showed that it resulted from mutual inductance between the aggressor and victim package pins. With a 250 mV edge with a rise time of 100 ps, less than 0.5 nH of mutual inductance causes this induced voltage. Three times the rise time with three times the swing (ECL swing with 300 ps rise time) will result in the same induced voltage.

The backward crosstalk shown has two components: the bump corresponding to the pin mutual inductance, and the crosstalk from the adjacent traces. The magnitude of the first bump is of opposite polarity to, but of similar duration to the measured (unexpected) forward cross talk - as is expected with inductive coupling. As expected, the duration of the second bump is 2 T_{prop}. With 250 mV swing of the TDR source, the measured backward crosstalk is also under 10%. The backward crosstalk is proportional to the swing of the aggressor, so an ECL swing should also result in 10% backward crosstalk.

5.5. Package Pin Via Capacitance

To study the sensitivity of pin capacitance to pin via design, the package incorporated three types of pin vias. Most pins used the normal via design preferred by the package vendor: each foil layer contained at least a circular pad of copper at the via site to facilitate accurate via hole drilling. After drilling, a small "annular ring" is left behind. The few minimum capacitance test vias contained no pads on unconnected signal layers and large clearances on to power planes. The few large capacitance test vias had large annular rings on signal layers which overlapped with the power planes (which had small clearances).

Figure 12 shows TDRs of a minimum, a maximum, and two normal pins. For each of the cases there are two overlaid traces, one for a package with a die, one without. These measure-

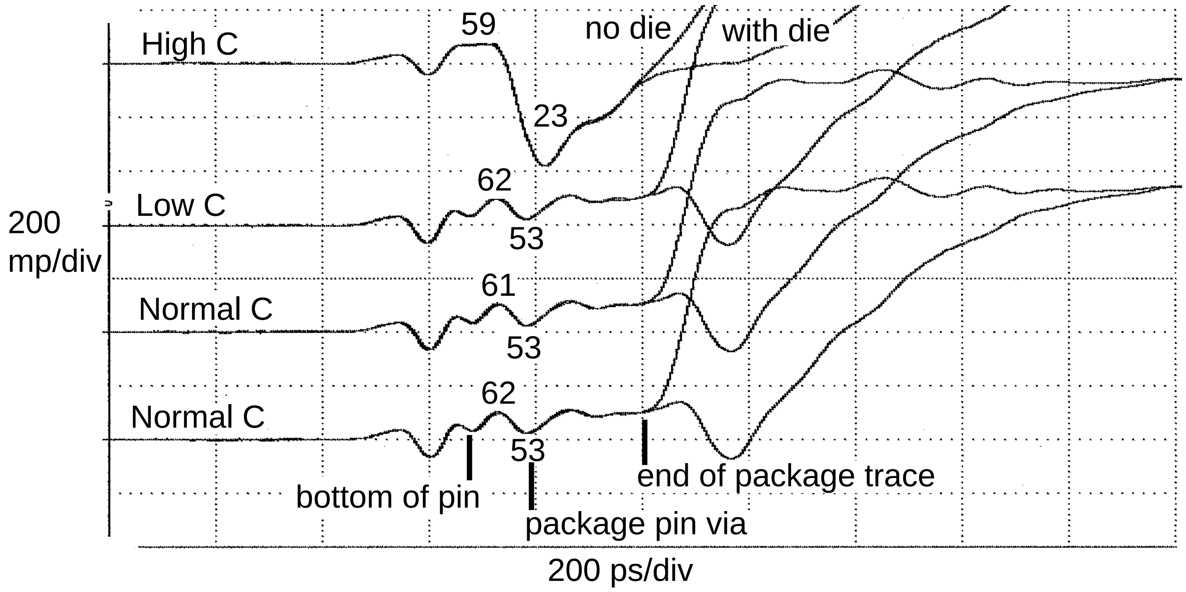

Figure 12: Pin Via Capacitance Sensitivity

ments show that is difficult to reduce the pin via capacitance, but that it is easy (but undesirable) to increase it.

5.6. Yet To Do: Simultaneous Switching Evaluation

Since almost all of the signal pins are single ended, simultaneous switching of outputs (SSO) and inputs (SSI) require evaluation.

Modeling the entire system of drivers, receivers, bond wires, and terminating resistors along with the power distribution system is beyond our expertise. The chip and package design techniques which were used to reduce the problems due to SSI and SSO are outlined below. We plan to measure the on-chip power supply noise and the effects of simultaneous switching on the actual BIPS chips.

SSI is not usually a problem, but for BIPS it requires consideration since there is on-chip termination and therefore potentially substantial termination current changes as the inputs change (about 25 mA per input). To isolate noise generated on the terminating voltage source from the rest of the chip, the terminating voltage (-2.2 V) was brought on to the chip from separate supply pins; it was not generated from Vee (-5.2 V) on-chip. The terminating voltage was bussed on-chip and supplied from a plane on the package. There was one bond wire for each 7 inputs. Pads for surface-mount bypass capacitors were provided on the package.

SSO usually requires consideration. The package contained a Vcc (ground) plane which supplied Vcc and Vcco (Vcc for the pad output drivers) to the chip. Vcco was separated from the Vcc for the rest of the chip by providing separate Vcc and Vcco bondwires (relying on the bondwire inductance to electrically isolate them) and not connecting Vcc and Vcco on-chip. Using a "black magic" technique which has worked in the past, Vcc and Vcco are AC coupled together to a common node (the negative supply) to prevent oscillation. This causes some noise on negative supply which has some small effect on the current sources. Vcco was bussed on-chip with one bond wire for each 3 or 4 outputs. Vcc and Vee were gridded on-chip in metal layers 3 and 4. Pads for surface-mount bypass capacitors were provided for Vcc on the package.

6. Conclusions

The performance of the BIPS-0 package is better than is required for the BIPS-0 chip and will suffice for BIPS-1. Use of the ZIF socket only slightly degrades the signals: the BIPS-0 package in a ZIF socket is capable of passing 150 ps rise time signals.

The package impedance is acceptable at 60 Ω and improvement is expected. Impedance discontinuities due to the PCB plated through holes, ZIF socket, pins, pin vias, traces, bond wires and chip I/O pads are all small and acceptable.

Crosstalk to an adjacent trace with a single signal switching was found to be under 10% and needs to be considered in the PCB signal noise budget.

The on-chip terminating resistors are great: electrically they work well (right resistance, no impedance discontinuities, no stubs) and their power dissipation is not a problem for the BIPS chips.

PCB-mounted SMA and Nanohex connectors perform inadequately for monitoring the few high-frequency analog test signals which are brought out from the BIPS chip onto the BIPS package. Instead future designs will provide lands on the package for standard Cascade 50 Ω microprobes on the packages.

The effects of simultaneous switching are yet to be determined.

7. Acknowledgements

Bill Hamburgen did a fine job designing this great package. Richard Evans provided guidance and assistance in this investigation.

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Table of Contents

List of Figures