Compaq Deskpro Workstation Maintenance & Service Guide

Maintenance & Service Guide Compaq Deskpro Workstation 300 Convertible Minitower Models and Compaq Deskpro EXS



LUMPAQ



System Unit

1	Power switch with cable, LED and switch holder [†]	223488-001
2	Power supply, 265 Watt	203430-001
*	Power supply, 265 Watt with PFC (EMEA only)†	224884-001
3	Access panel	Not spared
4	Front bezel †	221187-001
5	Chassis assembly	Not spared
6	Front bezel – Deskpro EXS only	225238-001
*Not shown.		

[†]Deskpro Workstation 300 only.

Mass Storage Devices

7	Diskette drive, 3.5-inch†	158266-001
*	Diskette drive, 3.5-inch (Deskpro EXS only)	123958-001
8	48X CD-ROM drive	187263-001
9	9.1-GB Hard drive [†]	160062-001
*	18.2-GB Hard drive [†]	160063-001
*	18.2-GB Hard drive [†]	194585-001
*	20-GB Hard drive [†]	180475-001
*	20-GB Hard drive [†]	157403-001
*	30-GB Hard drive [†]	180477-001
*	36-GB Hard drive †	167926-001
*	36.4-GB Hard drive [†]	192197-001
*	40-GB Hard drive (Deskpro EXS only)	202904-001
*	Zip Drive, 250-MB †	125776-001
*	Writeable CDRW Drive, 8/4/32x	101916-001
*	DVD-ROM Drive, 10x	215422-001
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Documentation (Not shown)

Maintenance and Service Guide	222098-001
Quick Troubleshooting Guide	153837-001
Service Reference Guide	225698-001

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First Edition. November 2000.

7



Spare Part Number: 222098-001



8



Keyboards - Deskpro EXS (Not shown)

Easy Access Keyboard-US	123130-xx1
Asia/Pacific	-37x
Australia	-B3x
Canada (French Canadian)	-05x
Japanese	-29x
Japanese (English)	-39x
U.S.	-00x

Keyboards - Deskpro Workstation 300 (Not shown)

Easy Access Keyboard-US	123130-xx1
Asia/Pacific	-37x
Europe	-A4x
French	-05x
German	-04x
Italian	-06x
Japanese	-29x
Japanese (English)	-39x
Korean	-ADx
Spanish	-07x
Swiss – English/Italian	-AHx
Swiss – French/German	-B5x
United Kingdom	-03x
U.S.	-00x
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Miscellaneous Plastics Kits

	Miscellaneous Plastics Kit, includes:	166878-001
21	Panel, sub (166835-001)	
22	Bezel, blank (166775-001)	
23	Diskette bezel (166776-001)	
24	Card guide (166778-001)	
25	Foot, rubber (4 ea.) (166939-002)	
26	Button, power (166774-001)	
27	Drivelock, DT (166779-001)	
28	Spring, power button (166837-001)	
29	Springs, drivelock (2 ea.) (166837-002)	
30	Drivelock, MT (166780-001)	
*	Retention mechanism (2 ea.) (350767-001)	
	Miscellaneous Plastics Kit, includes:	400549-001
*	Holder switch (166877-001)	
24	Card guide (166778-001)	
25	Foot, rubber (4 ea.) (166939-002)	
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*Not shown.

†Deskpro Workstation 300 only.

Cables

10	Diskette drive cable, 18"	221186-001
	Cable Kit, includes:	166879-002
*	Diskette drive cable with twist, 11", with pull tab, center polarization (143218-001)	
11	40-position IDE data cable, 12.5" (105876-001)	
12	IDE Ultra ATA dual device, hard drive/CD-ROM cable, 18", with pull tab, (108950-015)	
*	Dual-LED power cable (1 ea.) (387727-001)	
*	Switch mounting bracket (3 ea.) (166777-001)	
*	Diskette drive/tape cable, with twist, no key, 34" (356107-001)	
*	Diskette drive cable with twist, 11", without pull tab (387795-001)	
13	IDE Ultra ATA dual device, hard drive/ CD-ROM cable, 14"	170225-001
*	IDE Ultra ATA , hard drive/CD-ROM cable, 18"	225881-001
14	Audio cable, 21"	149806-001
*	Audio CD cable	387527-001
*	5-device LVD SCSI cable	158277-001

*Not shown.

Standard and Optional Boards

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15	NIC, 10/100 PCI, Intel PRO/100+	116188-001
*	NIC, 10/100 PCI, Intel PRO/100+, IPSEC †	215774-001
*	NIC, 10/100 PCI, 3Com 3C905C-TX, AOL †	118042-001
16	Nvidia TNT2 Pro 16-MB SDRAM AGP Controller †	179997-001
*	Nvidia Synergy II, 32-MB AGP Controller †	146140-001
*	Elsa GLoria II, 64-MB Graphics Controller †	174641-001
*	Matrox G450, AGP Graphics Controller †	203626-001
*	Nvidia Synergy III, 32-MB Graphics Card†	221492-001
*	Ultra3, PCI/SCSI Adapter Card†	158364-001
17	Heatsink with clip	225354-001
*	Processor, Intel P4, 1.4GHz/400MHz	221184-001
*	Processor, Intel P4, 1.5GHz/400MHz	221185-001
18	System board	221183-001
	Memory Modules (RIMM, 800MHz)	
19	64 MB	157108-001
*	128 MB †	157112-001
*	256 MB †	161454-001
20	CRIMM	158265-001
*	Modem, 56K, Controller-Based, PCI	157071-B21
*	Modem, 56K (Deskpro EXS only)	146803-001
*	Modem, V.90, International (Deskpro EXS only)	166358-002
*Not	shown.	

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†[Deskpro	Workstation	300	only.

*Not shown

Miscellaneous Parts

31	Air baffle	224205-001
32	Battery	153099-001
33	Mouse, scroll, opal	334689-001
*	Mouse, 3-button, opal †	327716-001
34	Speaker, 40mm x 70mm	180809-001
35	Fan, 92mm	158275-001
36	Drive adapter, 3.5-inch	180808-001
*	Return kit	207742-001

*Not shown. †Deskpro Workstation 300 only.



Connectors and Jumpers

CR500	P/S ON, 5V Aux LED
CR503	Power Button LED
CR514	3.3V Aux LED
E49	Clear Password Header (Installed = Enabled, Removed = Cleared)
SW50	Clear CMOS
P1	Power Supply Connector
P3	Microprocessor Power-In Connector
Р5	Power Button / HDD LED / Power-On LED Header
XBT1	Battery Retainer
XMM3&4	RIMM Slot 3&4, Channel B

P7	CD-In Connector
P8	Chassis Fan Connector
P10	Diskette Drive Connector
P11	Second Audio Connector
P12	SOS Connector (3Com NIC only)
P20	Primary IDE Connector
P21	Secondary IDE Connector
J20-24	PCI Slots 1-5 (J24=Slot 5)
J74	AGP Slot
U15	System ROM
XU1	Primary Processor Socket
XMM1&2	RIMM Slot 1&2, Channel A

System Interrupts (IRQ)

IRQ	System Function
0	Timer Interrupt
1	Keyboard
2	Interrupt Controller Cascade
3	Serial Port (COM B)
4	Serial Port (COM A)
5	Available for PCI
6	Diskette Drive
7	Parallel Port (LPT 1)

11	PCI Steering Input
12	Mouse
13	Coprocessor
14	Primary IDE Controller
15	Secondary IDE Controller

IRQ System Function

Real-Time Clock

Available for PCI 10 Available for PCI

System DMA

Hardware DMA	System Function
0	Unused
1	Unused
2	Diskette Drive
3	ECP Parallel Port LPT1 (Default; Alternate = DMA 0)
4	DMA Controller Cascading
5	Unused
6	Unused
7	Unused

System Memory Map

8

9

Size	Memory Address	System Function
512 KB	FFFFFFFFh to FFF80000	System ROM
2030 MB	FEDFFFFFh to 80000000h	PCI Memory Expansion
2047 MB	7FFFFFFFh to 00100000h	HOST or PCI Memory Expansion
128KB	000FFFFFh to 000E0000h	System ROM
128 KB	000DFFFFh to 000C0000h	PCI Option ROMs
128 KB	000BFFFFh to 000A0000h	Video RAM
640 KB	0009FFFFh to 00000000h	Base Memory

Clearing CMOS

The computer's configuration (CMOS) may occasionally be corrupted. If it does, it is necessary to clear the CMOS memory using push button switch SW50. This will reset CMOS values to factory defaults and will erase any customized information including passwords, asset numbers, and special settings. To clear and reset the configuration, perform the following procedure:

1. Prepare the computer for disassembly.



CAUTION: The power cord must be disconnected from the power source before pushing the Clear CMOS Button (NOTE: All LEDs on the board should be OFF). Failure to do so may damage the system board.

- 2. Remove the access panel.
- 3. Press the CMOS button located on the system board and keep it depressed for 5 seconds.
- 4. Replace the access panel and turn the computer on. 5. Run F10 Computer Setup to reconfigure the system.

ICH Fixed I/O Registers

00h, 02h, 04h, 06h	Register Name
	Channel 0, 1, 2, 3 DMA Base & Current Address Regsiter
C0h, C4h, C8h, CCh	Channel 4, 5, 6, 7 DMA Base & Current Address Register
01h, 03h, 05h, 07h	Channel 0, 1, 2, 3 DMA Base & Current Count Register
	•
C2h, C6h, Cah, CEh	Channel 4, 5, 6, 7 DMA Base & Current Count Register
10h-1Fh	Aliased at 00h-0Fh
20h	Master PIC ICW1 Init. Cmd Word 1 Register
	Master PIC OCW2 Op Ctrl Word 2 Register
	Master PIC OCW3 Op Ctrl Word 3 Register
21h	Master PIC ICW2 Init. Cmd Word 1 Register
	Master PIC ICW3 Init. Cmd Word 1 Register Master PIC ICW4 Init. Cmd Word 1 Register
	Master PIC OCW1 Op Ctrl Word 3 Register
24h-25h, 28-29h,	Aliased at 20h-21h
2Ch-2Dh, 30h-31h,	
34h-35h, 38h-39h,	
3Ch-3Dh	
40h	Counter O Interval Time Status Byte Format
	Counter 0 Counter Access Port Register
41h	Counter 1 Interval Time Status Byte Format
	Counter 1 Counter Access Port Register
42h	Counter 2 Interval Time Status Byte Format
	Counter 2 Counter Access Port Register
43h	Timer Control Word Register
	Timer Control Word Register Read Back
	Counter Latch Command
50h-53h	Aliased at 40h-43h
61h	NMI Status and Control Register
70h	
/ 011	NMI Enable Register Real-Time Clock (Standard RAM) Index Register
71h	Real-Time Clock (Standard RAM) Target Register
72h	Extended RAM Index Register
73h	Extended RAM Target Register
74h-75h	Aliased at 70h-71h
76h-77h	Aliased at 72h-73h or 70h-71h
80h, 84h-86h, 88h	Reserved Page Registers
81h, 82h, 83h	Channel 2, 3, 1 DMA Memory Low Page Register
89h, 8Ah, 8Bh	Channel 6, 7, 5 DMA Memory Low Page Register
0911, 0A11, 0D11	channel 0, 7, 5 DMA Memory Low Page Register
8CH-8Eh	Reserved Page Registers
8Fh	Refresh Low Page Register
91h-9Fh (except 92h)	Aliased at 81h-8Fh
92h	Fast A20 and INIT Register
A0h	Slave PIC ICW1 Init. Cmd Word 1 Register
	Slave PIC OCW2 Op Ctrl Word 2 Register Slave PIC OCW3 Op Ctrl Word 3 Register
	, ,
A1	Slave PIC ICW2 Init. Cmd Word 2 Register
	Slave PIC ICW3 Init. Cmd Word 3 Register Slave PIC ICW4 Init. Cmd Word 4 Register
	Slave PIC OCW1 Op Ctrl Word 1 Register
A4h-A5h, A8h-A8h,	Aliased at A0h-A1h
ACh-ADh, B0h-B1h,	
B4h-B5h, B8h-B9h,	
BCh-BDh	
B2h	Advanced Power Management Control Port Register
B3h	Advanced Power Management Status Port Register
COD CAD CRD CCD	Channel 4, 5, 6, 7 DMA Base and Current Address Register
C0h, C4h, C8h, CCh	
C1h	Aliased at C0h
C5h	Aliased at C4h
C9h	Aliased at C8h
CDh	Aliased at CCh
C2h, C6h, CAh, CEh	Channel 4, 5, 6, 7 DMA Base and Current Count Register
C3h	Aliased at C2h
C7h	Aliased at C6h
CBh	Aliased at CAh
CFh	Aliased at Ceh
	Channel 4-7 DMA Command Register
D0h	Channel 4-7 DMA Status Register
D0h	Aliased at D0h
D1h	
	Channel 4-7 DMA Write Single Mask Register
D1h	
D1h D4h	Channel 4-7 DMA Write Single Mask Register
D1h D4h D5h D6h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register
D1h D4h D5h D6h D7h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h
D1h D4h D5h D6h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register
D1h D4h D5h D6h D7h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h
D1h D4h D5h D6h D7h D8h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register
D1h D4h D5h D6h D7h D8h D9h DAh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register
D1h D4h D5h D6h D7h D8h D9h DAh DBh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh
D1h D4h D5h D6h D7h D8h D9h DAh DBh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register
D1h D4h D5h D6h D7h D8h D9h DAh D8h DBh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh
D1h D4h D5h D6h D7h D8h D9h DAh D9h DAh DBh DCh DEh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh
D1h D4h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Vrite All Mask Register
D1h D4h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh
D1h D4h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Vrite All Mask Register
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register
D1h D4h D5h D5h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Command Block Offset for Primary Drive
D1h D4h D5h D5h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary
D1h D4h D5h D5h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Command Block Offset for Primary Drive
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive PIO Mode Control Block Offset for Primary Drive
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive PIO Mode Control Block Offset for Primary Drive
D1h D4h D5h D5h D6h D7h D8h D9h D4h D6h D6h D6h D6h D6h D6h D7h 170h-177h 1F0h-1F7h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h 4D1h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Secondary Drive 376h PIO Mode Control Block Offset for Primary Drive Master PIC Edge/Level Triggered Register Slave PIC Edge/Level Triggered Register Slave PIC Edge/Level Triggered Register
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h 4D1h 400-47F CF9h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive Master PIC Edge/Level Triggered Register Slave PIC Edge/Level Triggered Register Super I/O Reset Control Register
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h 4D0h 400-47F CF9h F800-F87F	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive PIO Mode Control Block Offset for Primary Drive Master PIC Edge/Level Triggered Register Slave PIC Edge/Level Triggered Register Super I/O Reset Control Register Reserved (power management)
D1h D4h D5h D5h D6h D7h D8h D9h DAh DBh DCh DEh DEh DFh F0h 170h-177h 1F0h-1F7h 3F6h 4D0h 4D1h 400-47F CF9h	Channel 4-7 DMA Write Single Mask Register Aliased at D4h Channel 4-7 DMA Channel Mode Register Aliased at D6h Channel 4-7 DMA Clear Byte Pointer Register Aliased at D8h Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Master Clear Register Aliased at DAh Channel 4-7 DMA Clear Mask Register Aliased at DCh Channel 4-7 DMA Write All Mask Register Aliased at DEh Coprocessor Error Register PIO Mode Command Block Offset for Secondary PIO Mode Control Block Offset for Primary Drive 376h PIO Mode Control Block Offset for Primary Drive Master PIC Edge/Level Triggered Register Slave PIC Edge/Level Triggered Register Super I/O Reset Control Register

Disabling or Clearing the Power-On and Set-up Passwords

- 1. Turn off the computer and any external devices, and disconnect the power cord from the power outlet.
- 2. Remove the access panel.
- 3. Locate the header and jumper labeled E49.
- 4. Remove the jumper from pins 1 and 2. Place the jumper over pin 2 only, in order to avoid losing it.
- 5. Plug in the computer and turn on power. Allow the operating system to start. This clears the current passwords and disables the password features.
- 6. Re-enable the password features by repeating steps 1-3, and then replacing the jumper on pins 1 and 2.
- 7. Replace the access panel.

Refer to the Computer Setup (F10 Setup) instructions to establish new passwords.

CMOS Archive and Restore (Power Switch Override)

Each time the system starts, the system ROM saves a copy of NVRAM (including CMOS, passwords, and other system variables) in the flash ROM. Should the system become unstable, the last known good copy of NVRAM can be restored using a feature called "power button override." To restore NVRAM, do the following:

- 1. With the unit powered down, press and release the power button.
- 2. Immediately after pressing the power button (during POST), press and hold the power button until the unit powers down (about 4 seconds).

At the next startup, the ROM detects this "power button override" event and the backup copy of NVRAM is restored.

Because of this feature, users cannot power off the computer immediately after powering up. The video display must be active before the computer can be powered off.



CAUTION: Unplugging the power cord during POST can corrupt the splash screen. Flashing the ROM is required to restore the splash screen. The computer will continue to function even if the splash screen has been corrupted.

NOTE: When the POS_DEC_EN bit is set, additional I/O ports get positively decoded by the ICH.